



MS-7119 Ver:0A

CPU: Socket A for AMD Athlon XP (K7)

System Chipset:
NFORCE2 IGP-64
MCP2SL (South Bridge)

On Board Chipset:
LPC Super I/O -- W83627THF Ver:
LAN -- PHY RTL8201CL
AC'97 Codec --ALC655

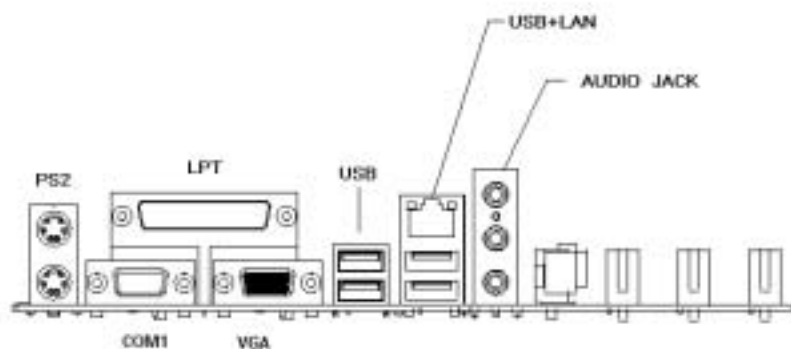
BIOS --LPC FLASH ROM

CLOCK Chip :
CLOCK Generator -- ICS950917AF

Main Memory:
DDR * 2 Support DDR400/333/266

Expansion Slots:
PCI2.3 SLOT * 3
CNR SLOT * 1

PWM:
NIKO N2101



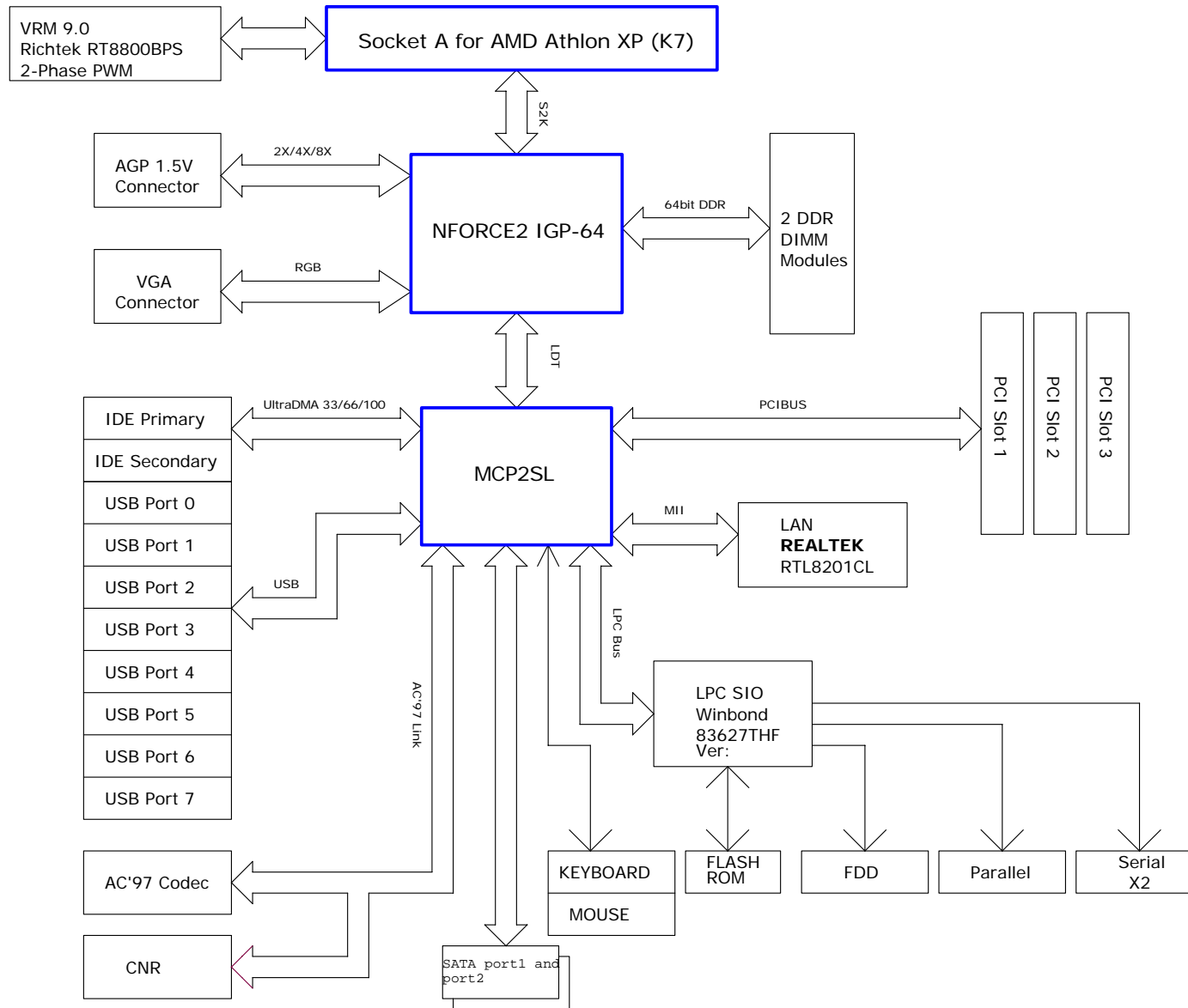
CHIPSET NFORCE2 IGP-64 + MCP2SL

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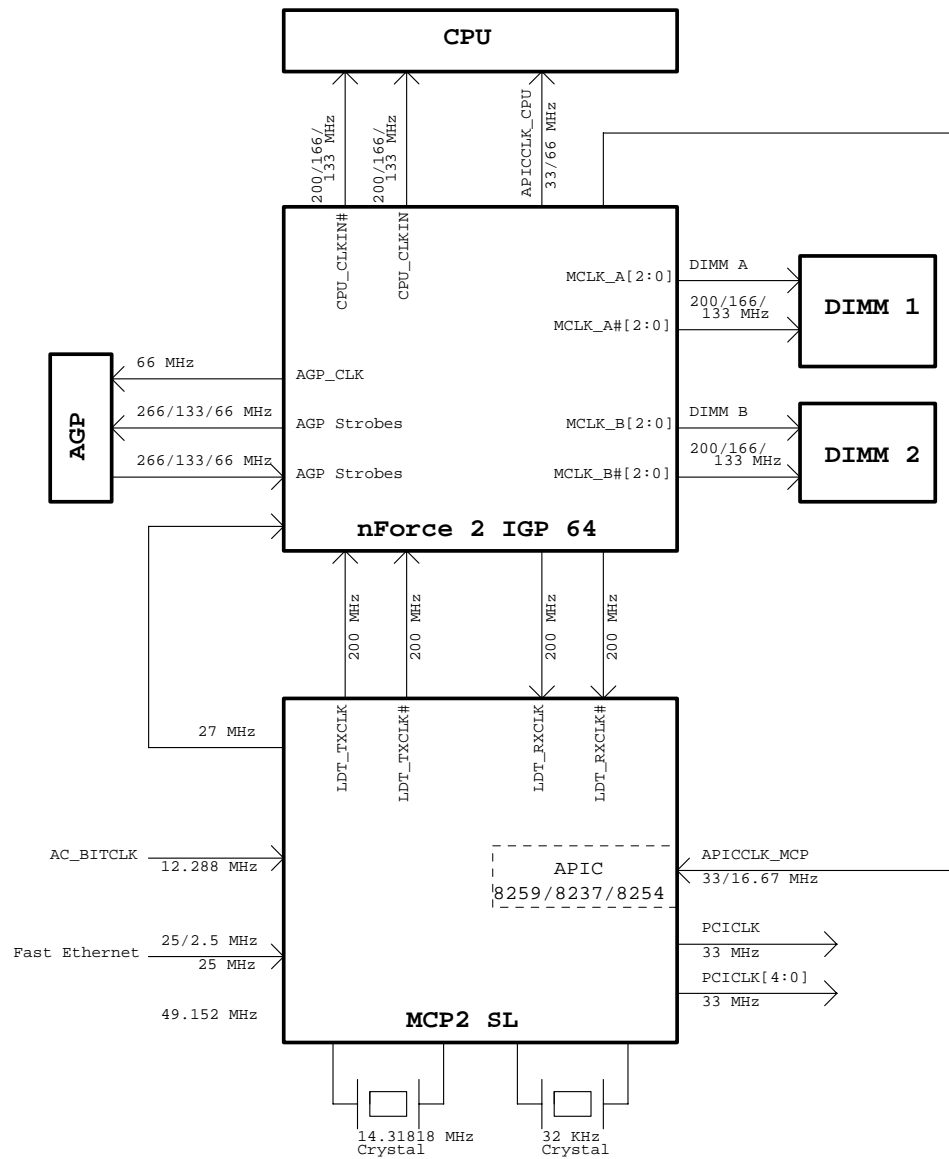


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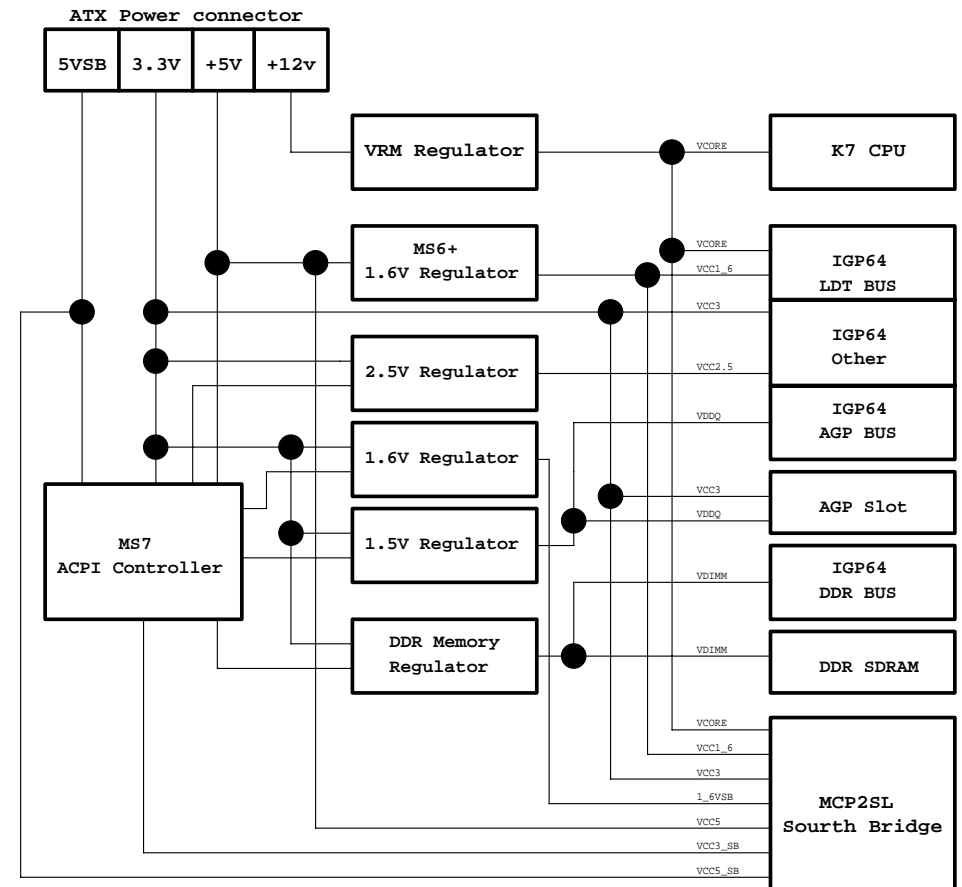
Block Diagram



NFORCE 2 IGP-64 PLATFORM CLOCK MAP



NFORCE 2 IGP-64 PLATFORM POWER DELIVERY MAP



[illegible]

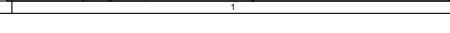
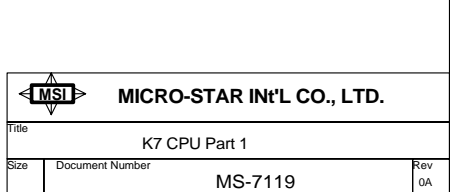
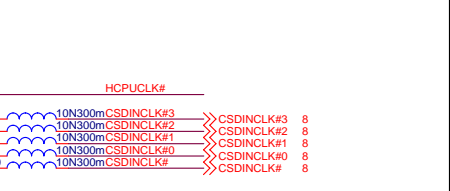
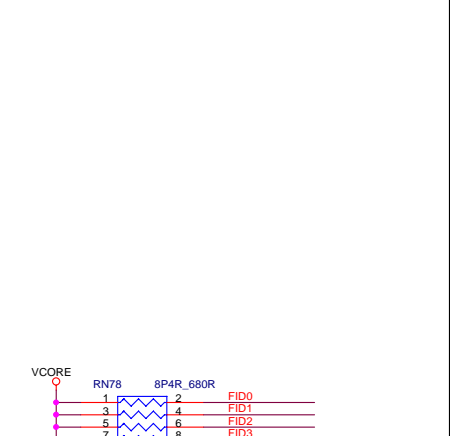
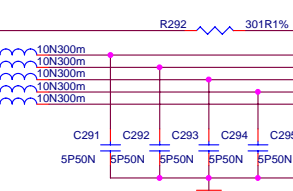
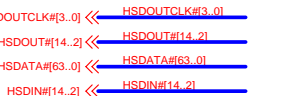
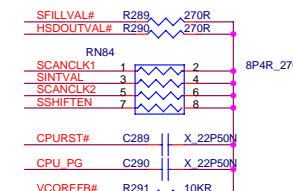
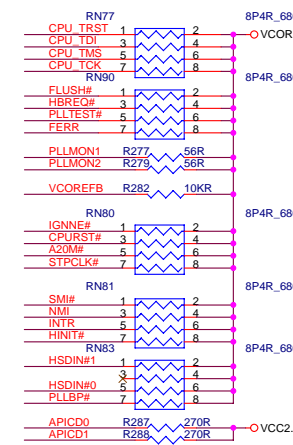
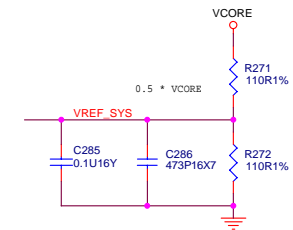
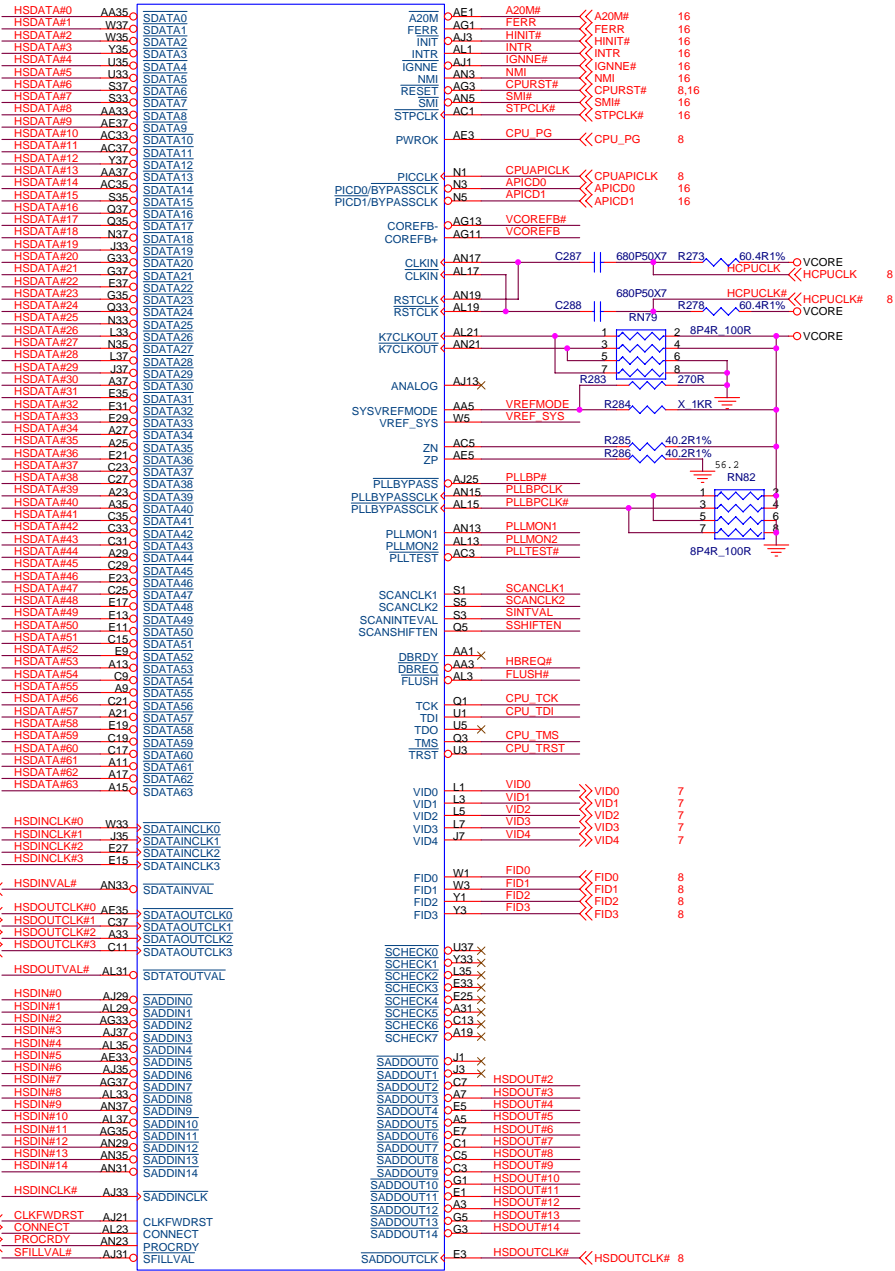
USB		Port	DATA +/-	OC#
Rear	USB1	USBP0+ USBN0- USBP1+ USBN1-	USB_OC#1	
	LAN_USB1A	USBP2+ USBN2- USBP3+ USBN3-		
Front	JUSB1	USBP4+ USBN4- USBP5+ USBN5-	USB_OC#3	
	JUSB2	USBP6+ USBN6- USBP7+ USBN7-		

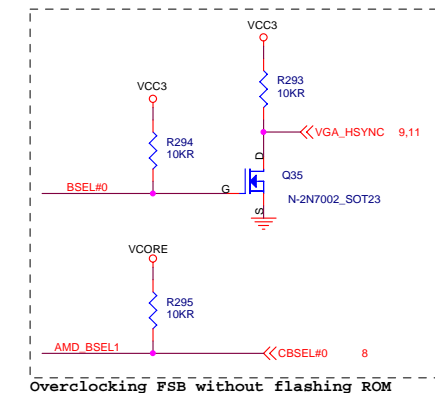
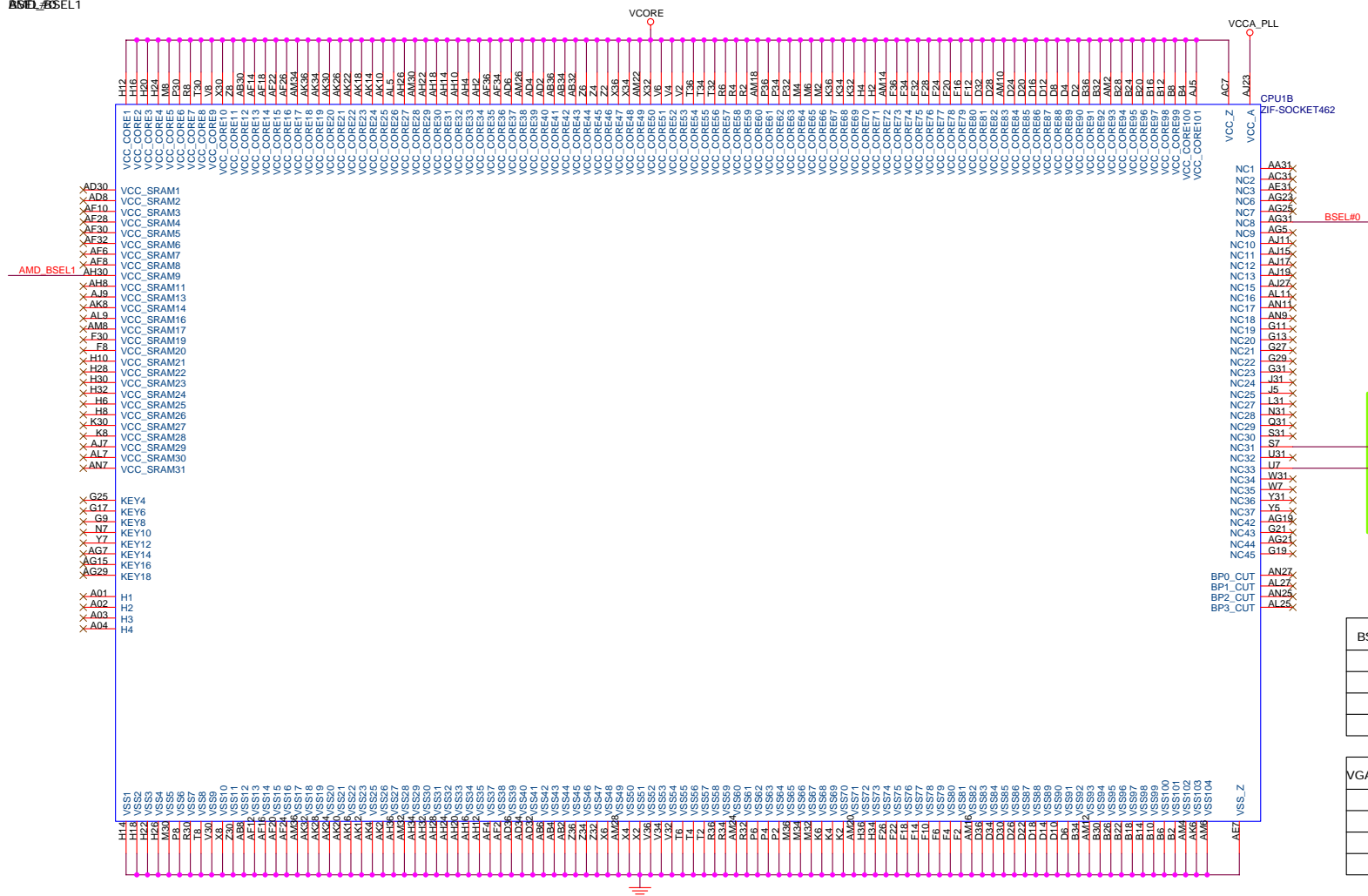
Signals	Target
PCIRST#	MS7
PCIRST#1	SIO, BIOS
PCIRST#2	PCI slot 1-3
PCIRST#4	AGP Slot, NB
HD_RST#	Primary, Scondary IDE

Signals	Target
SMBCLK0	Memory
SMBCLK1	MS7

DEVICE	MCP2 INT Pin	REQ#/GNT#	IDSEL	CLOCK
PCI Slot 1	INTC# INTD# INTA# INTB#	PREQ#0 PGNT#0	AD22	PCICLK0
PCI Slot 2	INTD# INTA# INTB# INTC#	PREQ#1 PGNT#1	AD23	PCICLK2
PCI Slot 3	INTA# INTB# INTC# INTD#	PREQ#2 PGNT#2	AD24	PCICLK3

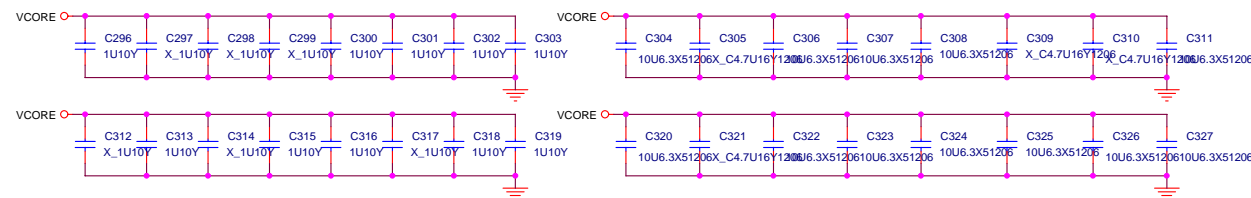
DEVICE	ADDRESS	CLOCK
DIMM 1	(A0) 1010000B	MDCLKA0/MDCLKA#0
		MDCLKA1/MDCLKA#1
		MDCLKA2/MDCLKA#2
DIMM 2	(A1) 1010001B	MDCLKB0/MDCLKB#0
		MDCLKB1/MDCLKB#1
		MDCLKB2/MDCLKB#2

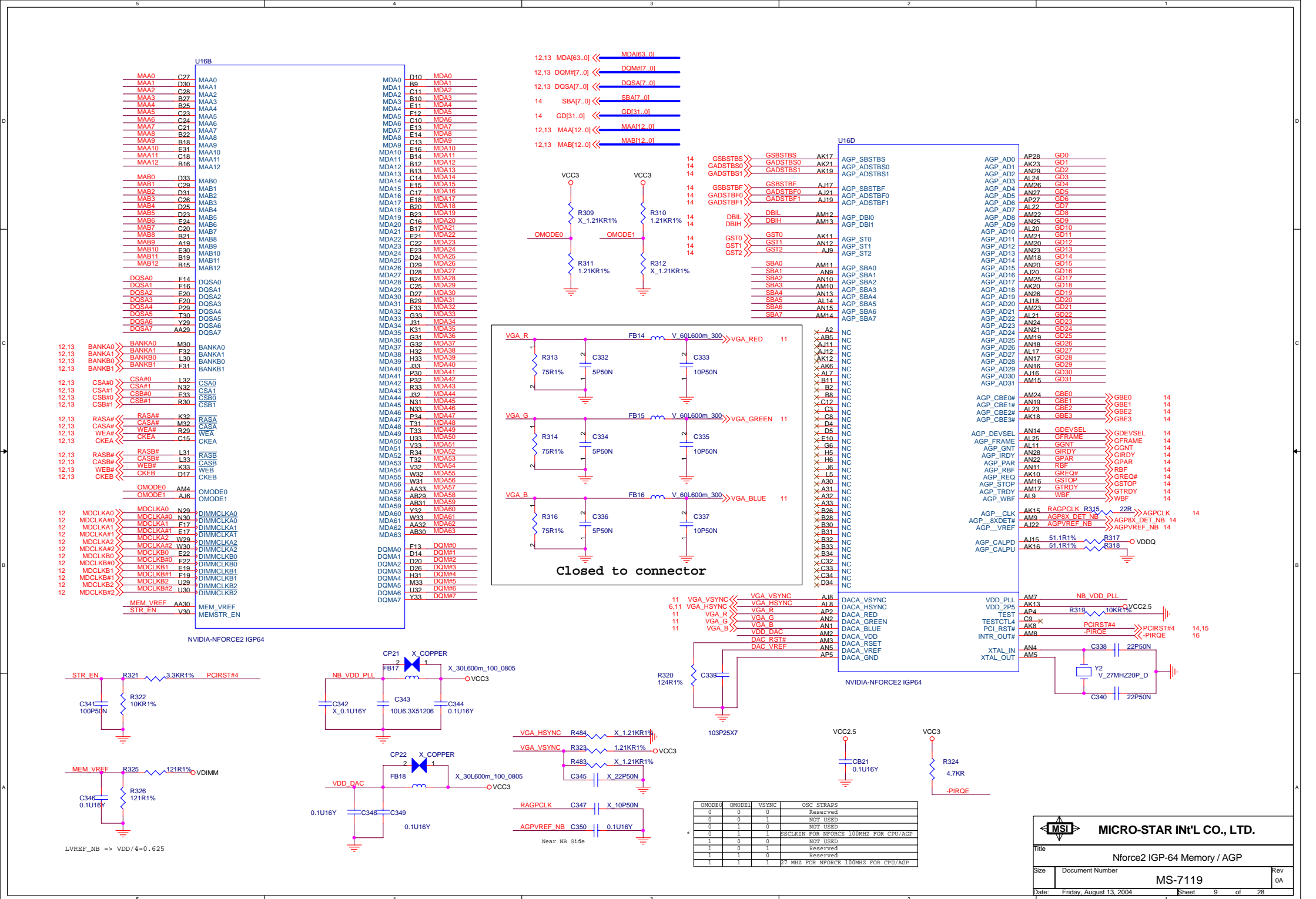


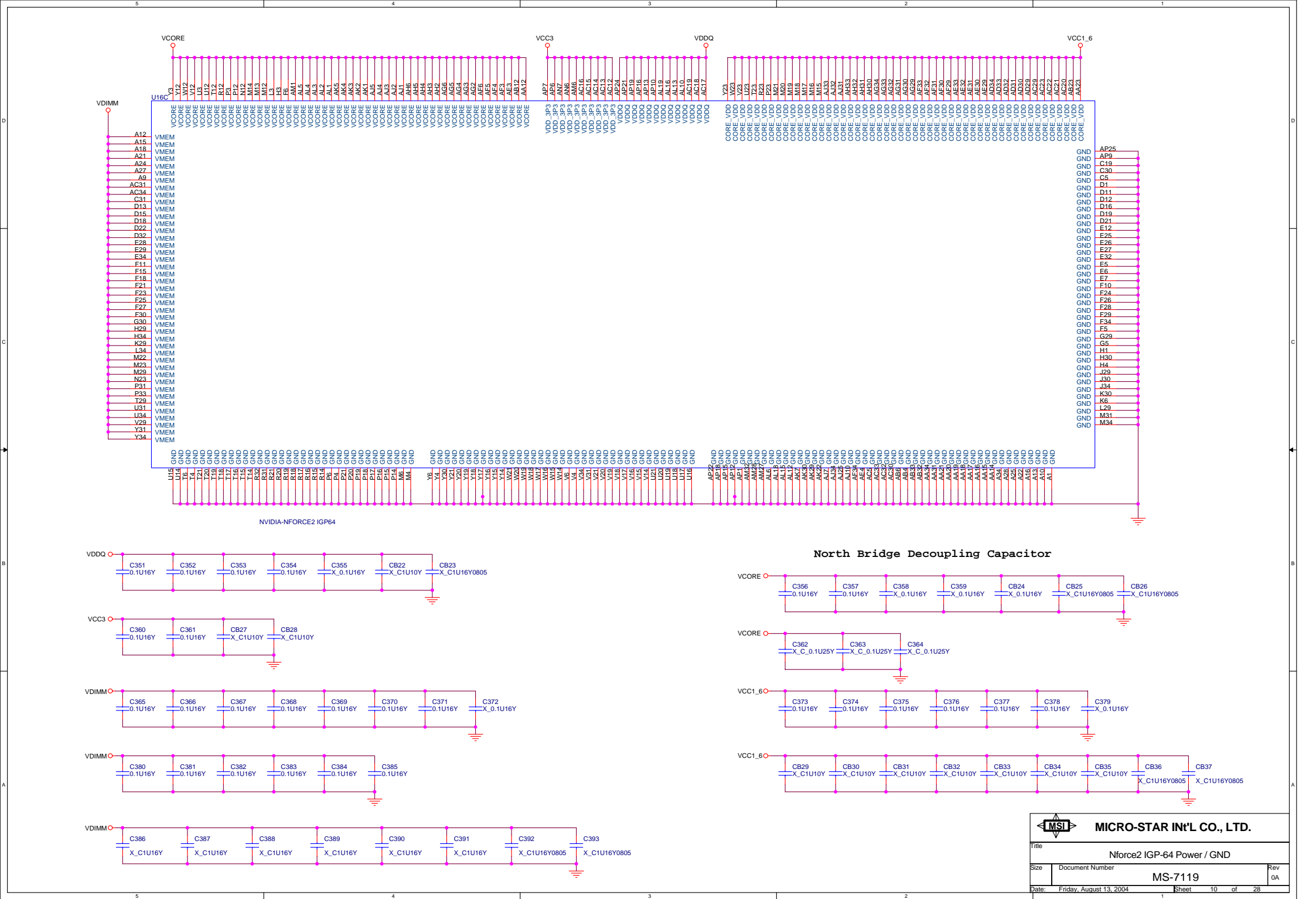


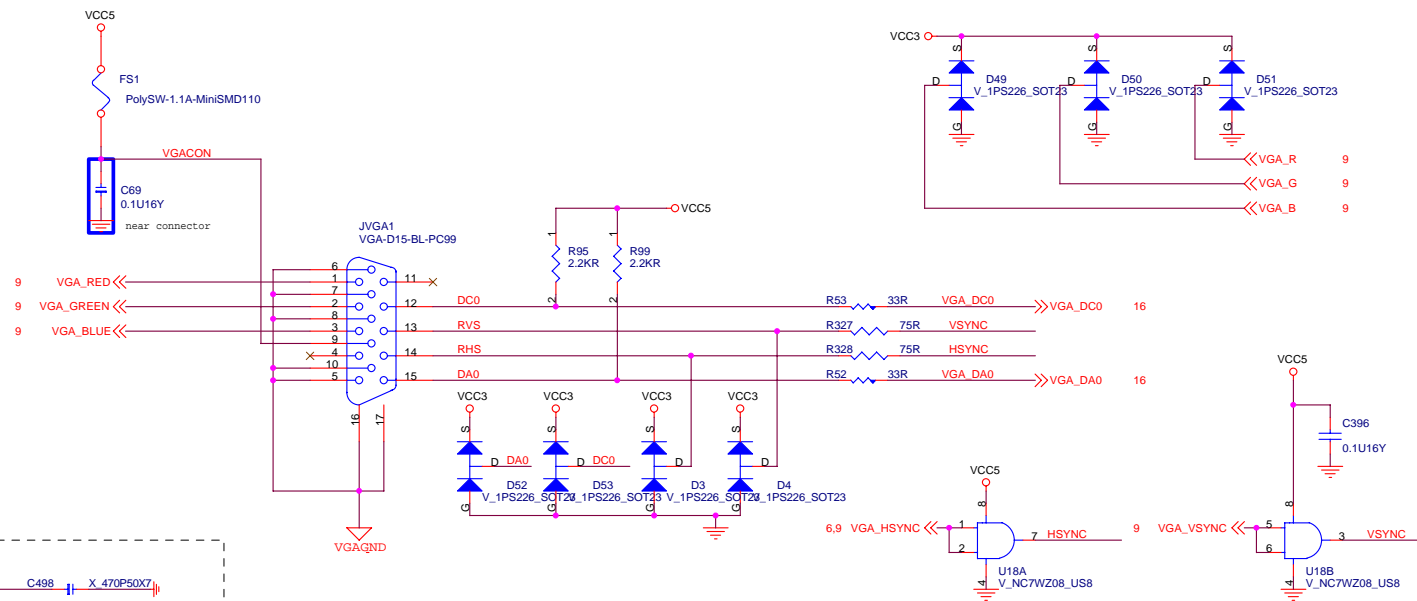
BSEL#0	AMD_BSEL1	CPU FREQUENCY
0	0	200 MHZ
1	0	166 MHZ
1	1	133 MHZ
0	1	RESERVED

VGA_HSYNC	CBSEL#0	FSB	Pointer location
1	0	200	0xFFFF_FFE4
0	0	166	0xFFFF_FFE0
0	1	133	0xFFFF_FFE8
1	1	N/A	0xFFFF_FFEC



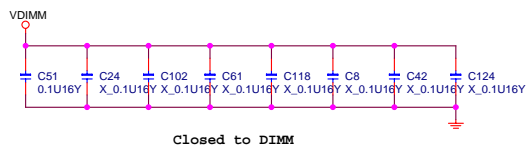
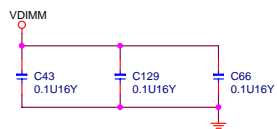
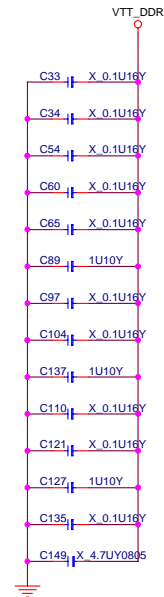
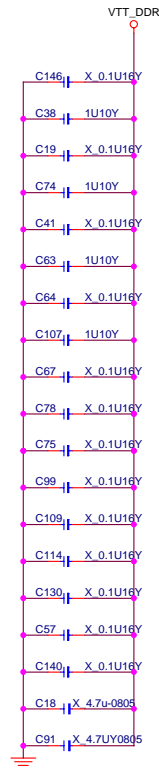
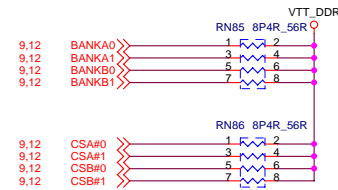
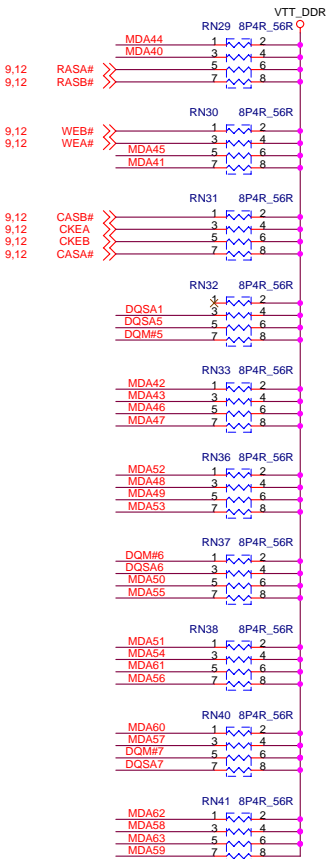
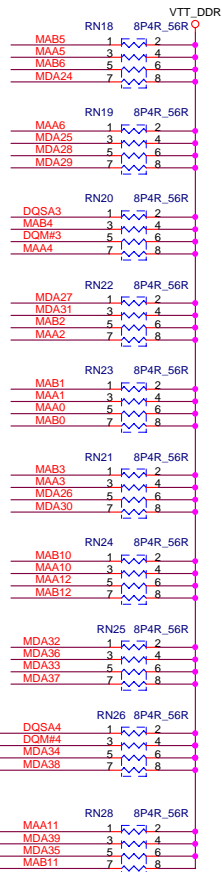
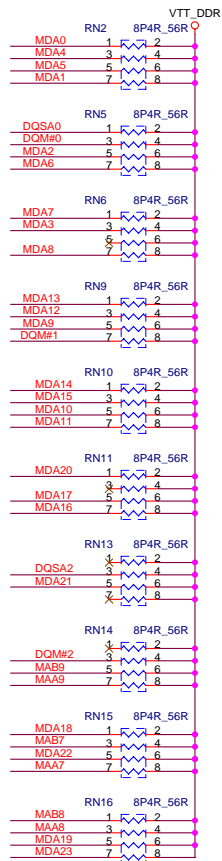


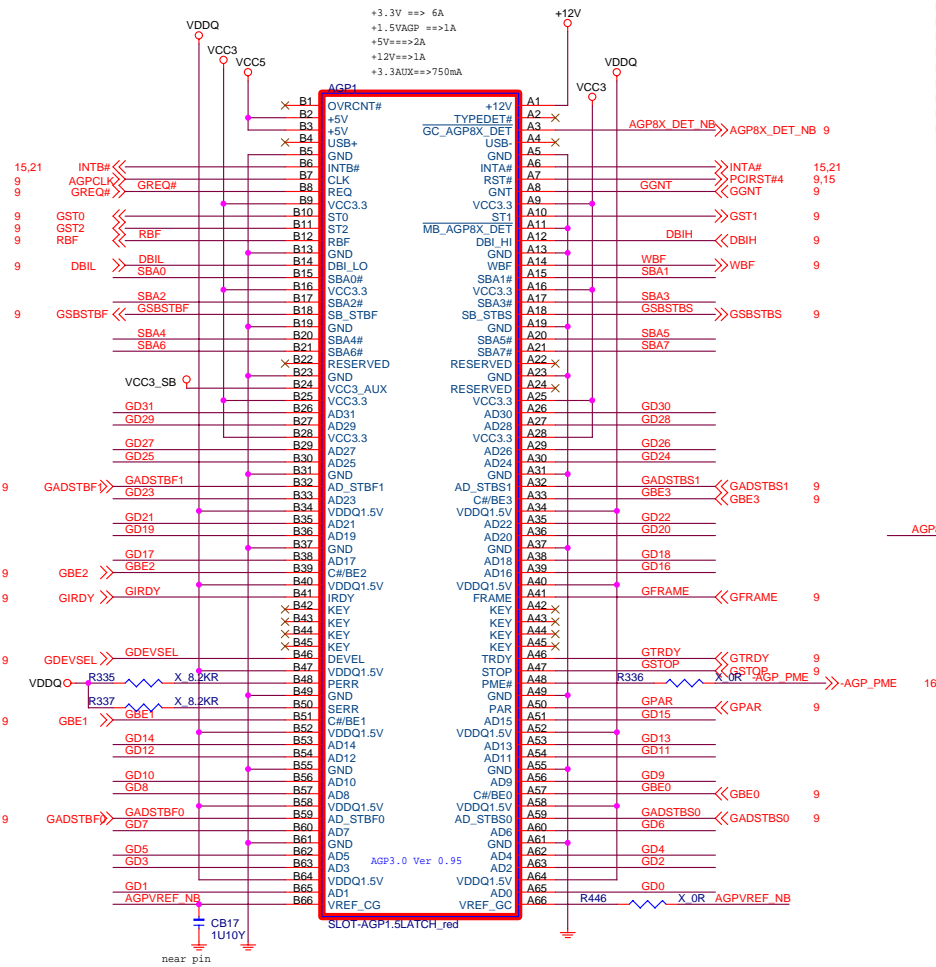




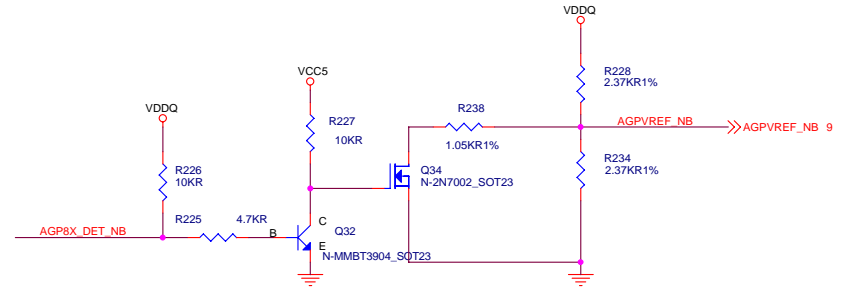
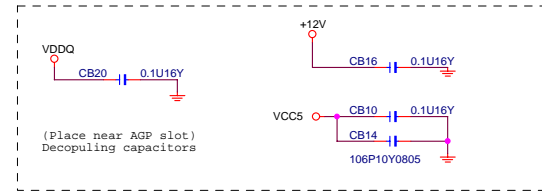
MDA[63..0] << MDA[63..0] 9,12
DQM#[7..0] << DQM#[7..0] 9,12
DQSA[7..0] << DQSA[7..0] 9,12

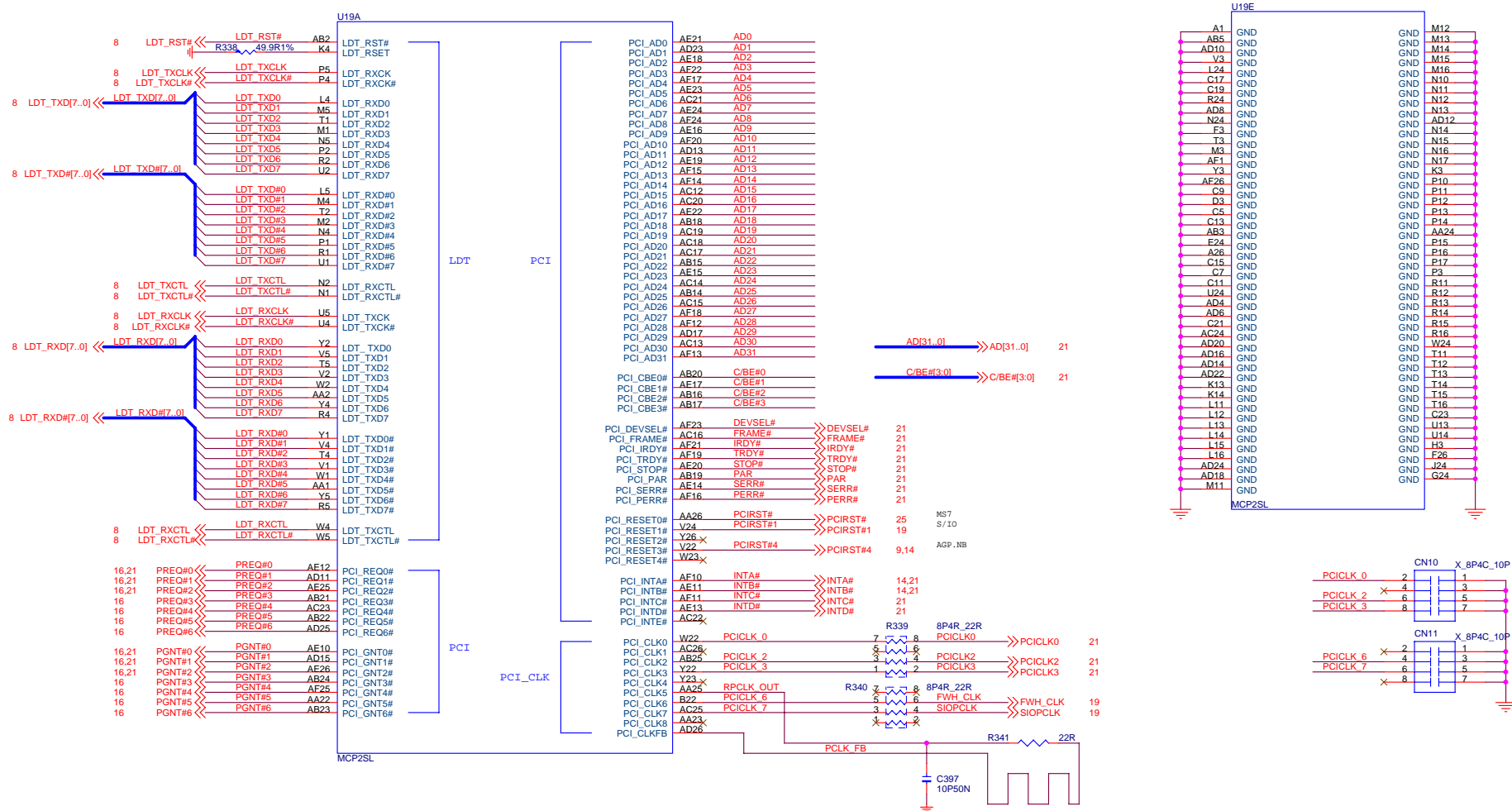
MAB[12..0] >> MAB[12..0] 9,12
MAA[12..0] >> MAA[12..0] 9,12

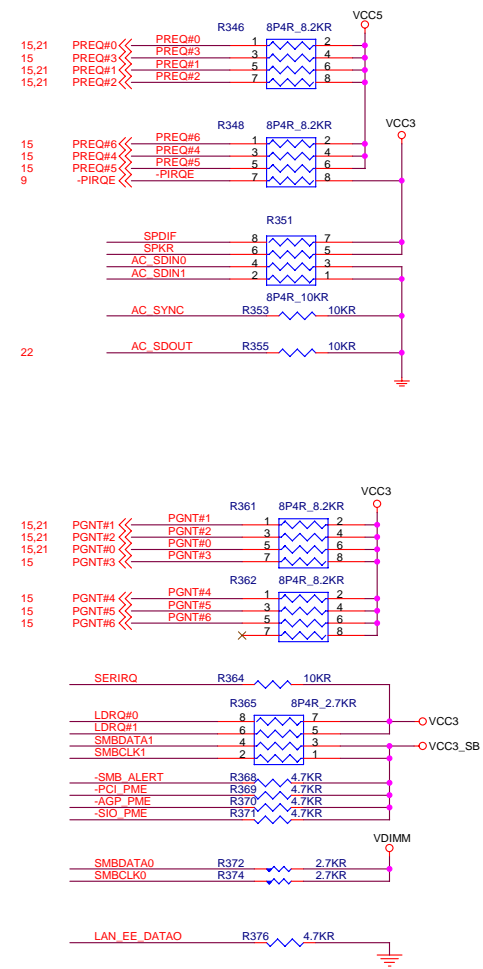
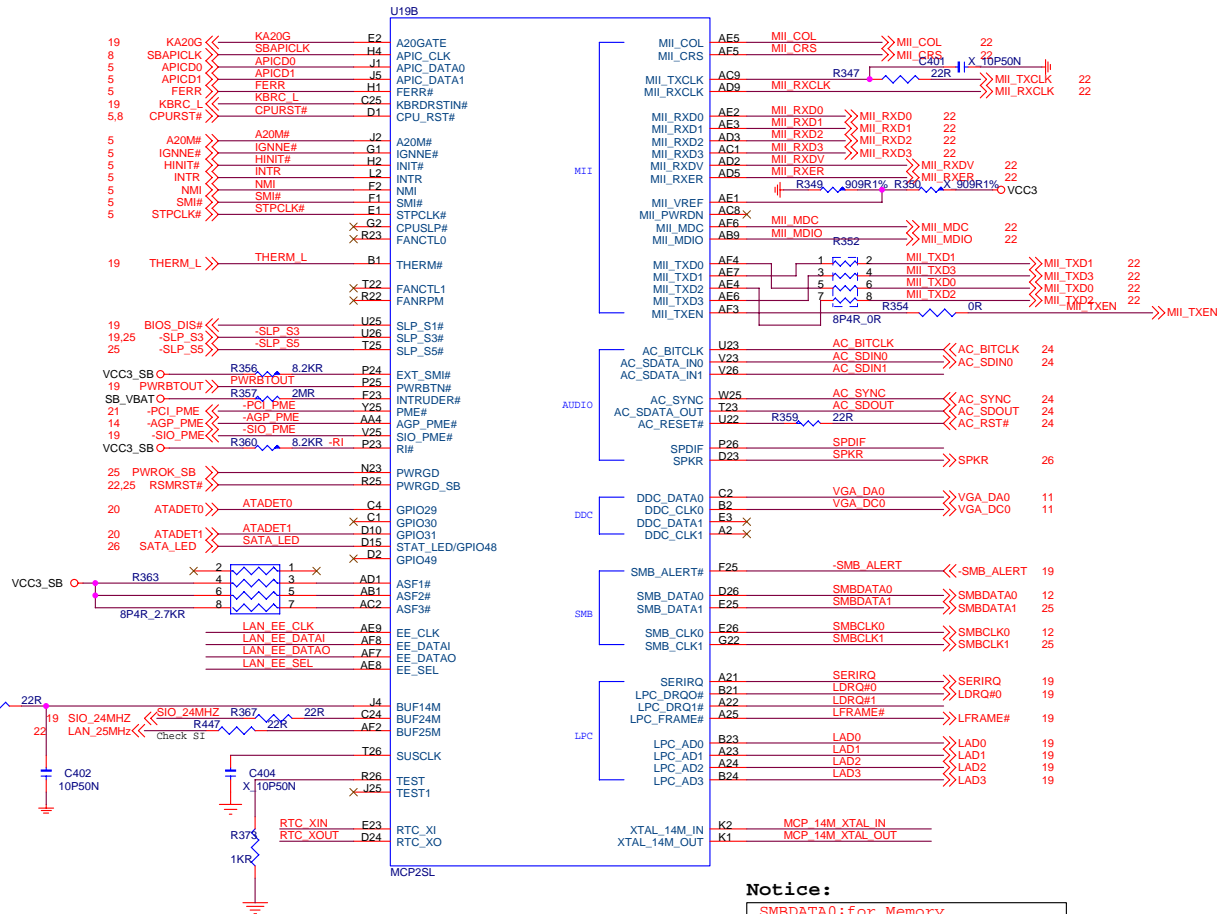




SBA[7..0] >> SBA[7..0] 9
GD[31..0] >> GD[31..0] 9

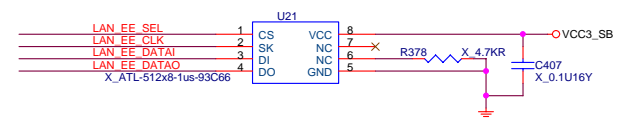


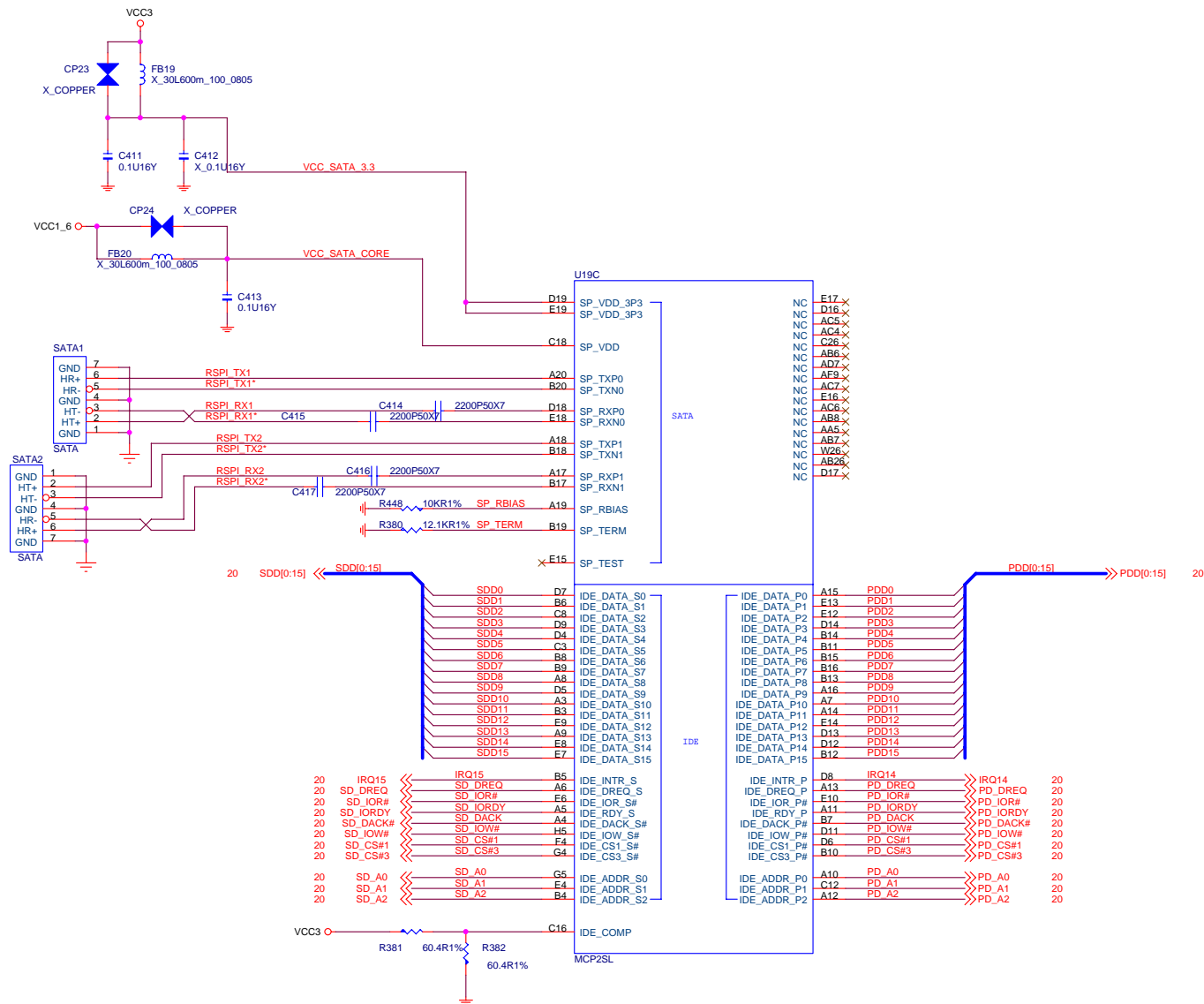


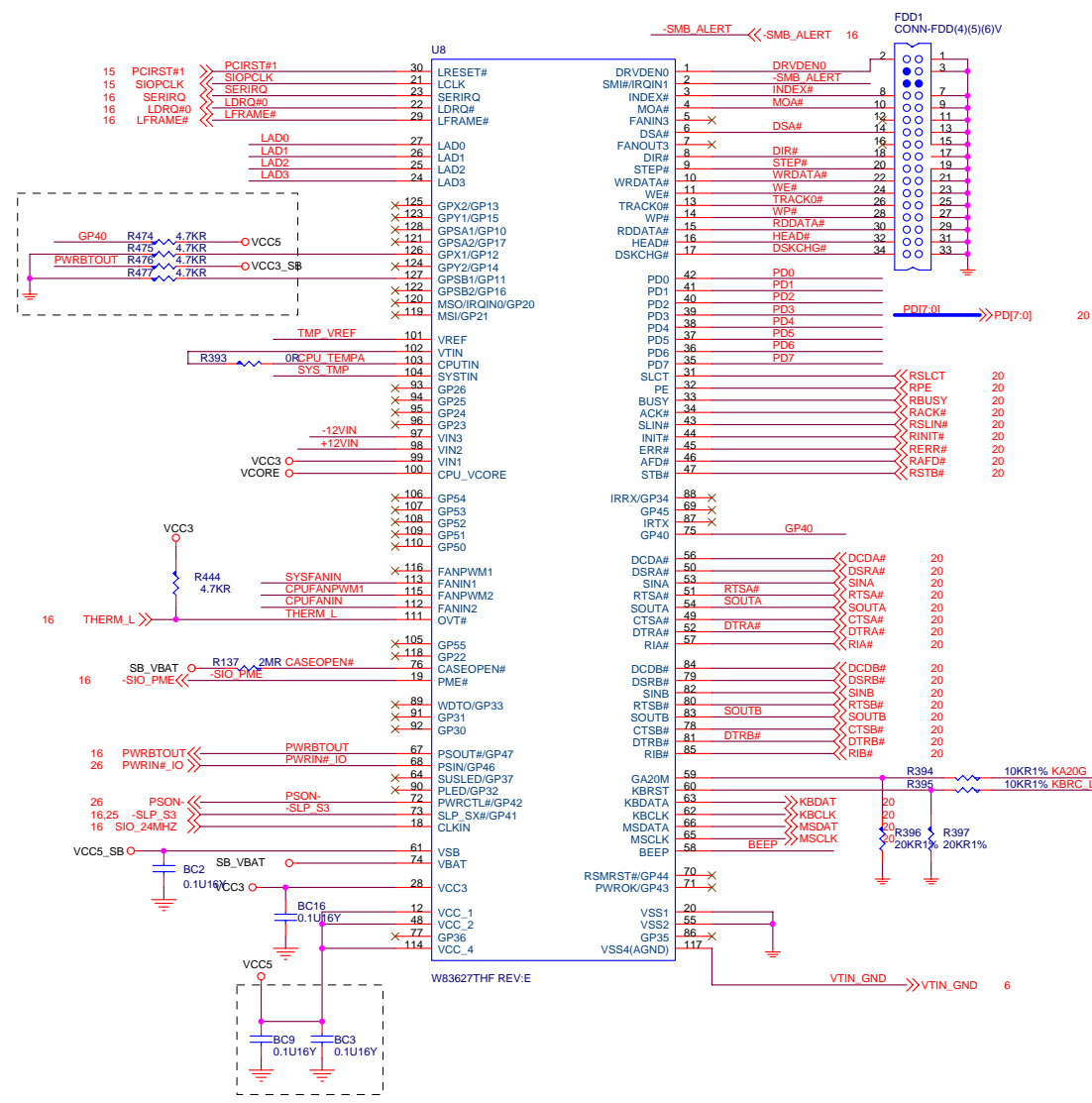


Notice:
 SMBDATA0: for Memory
 SMBDATA1: for PCI Slot, CNR, SIO

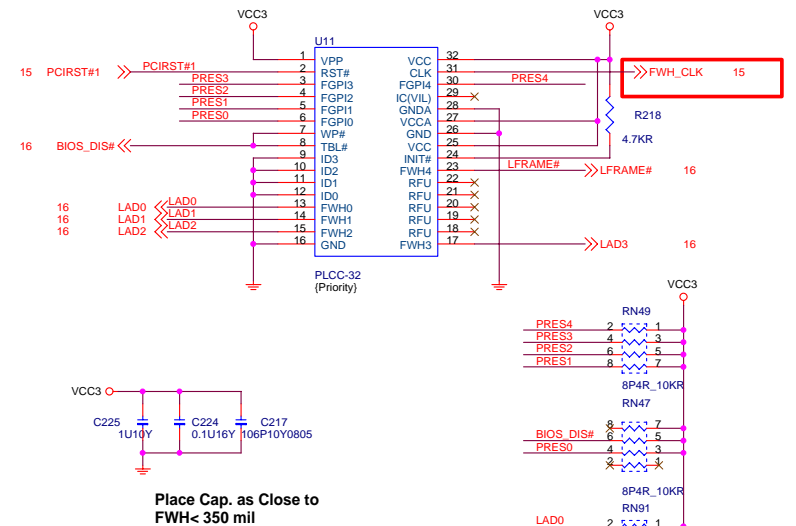
MCP2SL STRAPS	DEFAULT
SPKR	HIGH
SPDIF	HIGH
AC_SDATA_OUT	LOW
AC_SYNC	LOW
EE_DATA_OUT	LOW





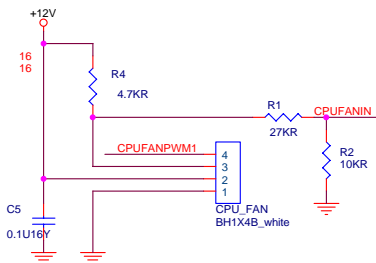


Flash ROM

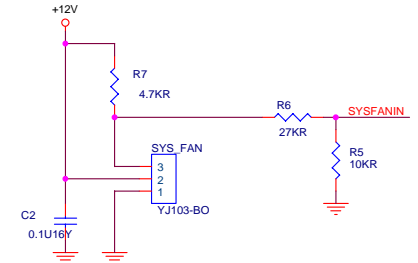


Place Cap. as Close to FWH< 350 mil

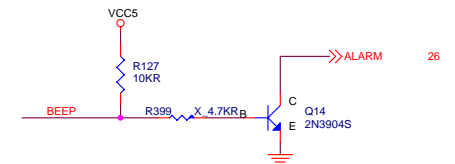
CPU FAN



SYS FAN



SPEAKER BLOCK

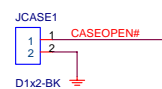


Straps

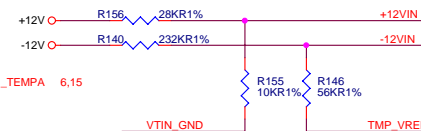


SOUTA	L: Disable KBC	H: Enable KBC
SOUTB	L: 24MHZ	H: 48MHZ
RTSA#	L: CFAD=2E	H: CFAD=4E
DTRA#	L: PNP Default	H: PNP no Default

Chassis Intrusion



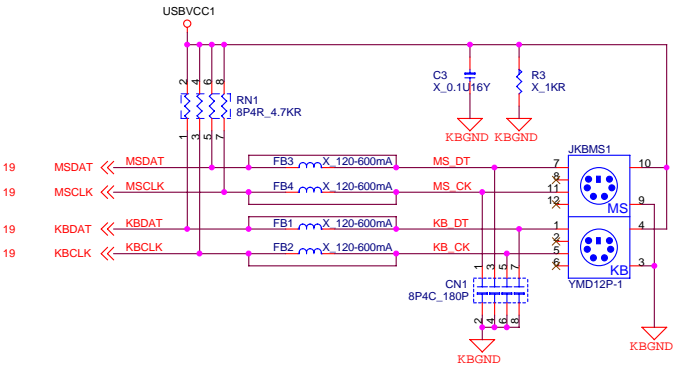
Hardware Monitor



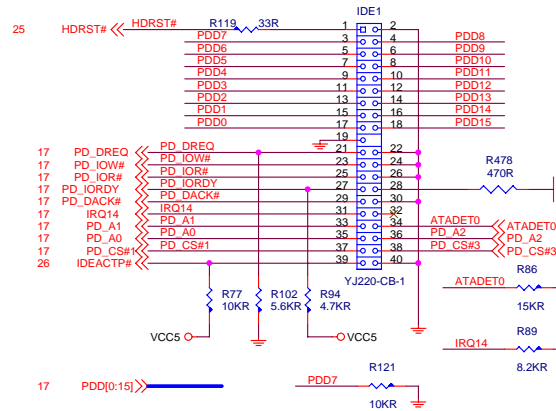
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Title	W83627THF-E SIO / Flash ROM	
Size	Document Number	Rev
	MS-7119	0A
Date:	Friday, August 13, 2004	Sheet 19 of 28

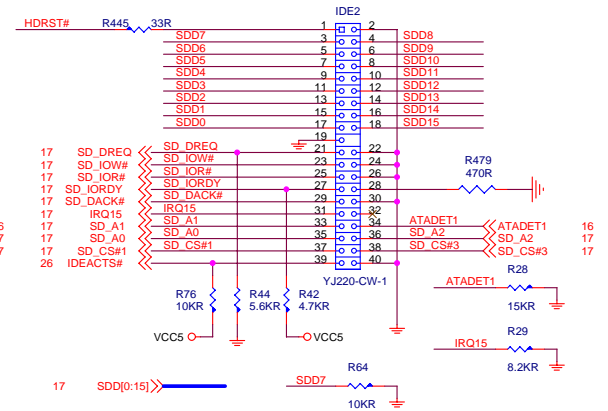
PS2 KEYBOARD & MOUSE CONNECTOR



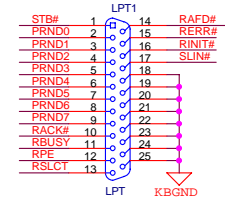
PRIMARY IDE BLOCK



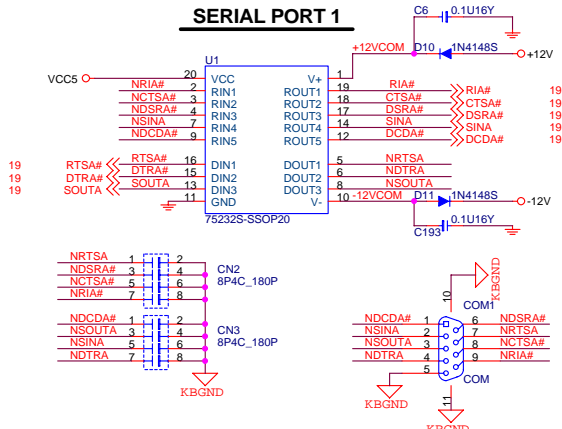
SECONDARY IDE BLOCK



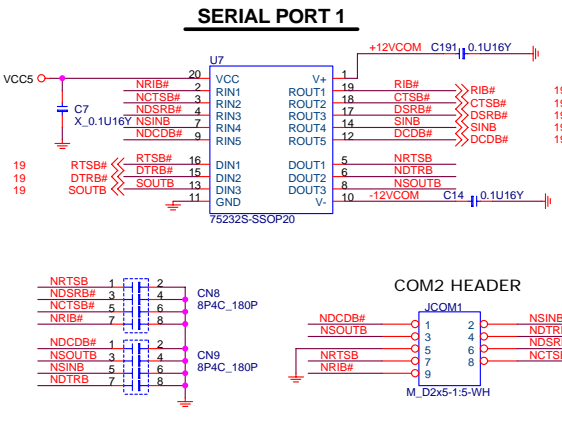
PARALLEL PORT



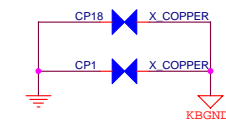
SERIAL PORT 1



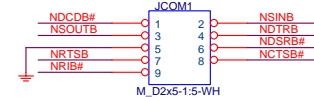
SERIAL PORT 1



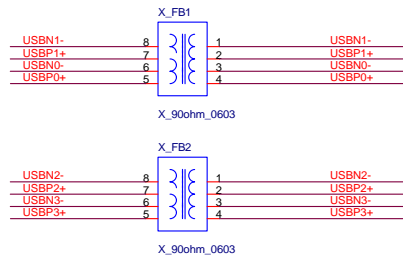
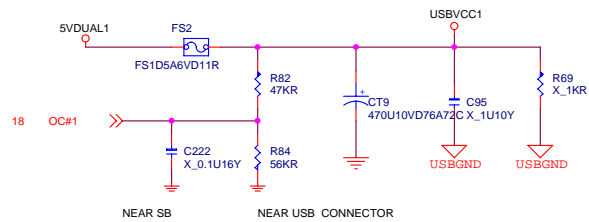
EMI



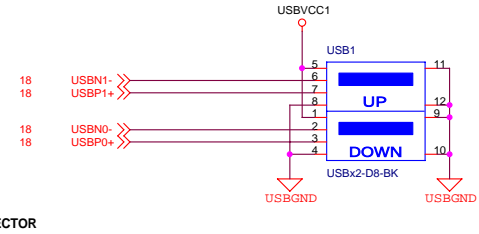
COM2 HEADER



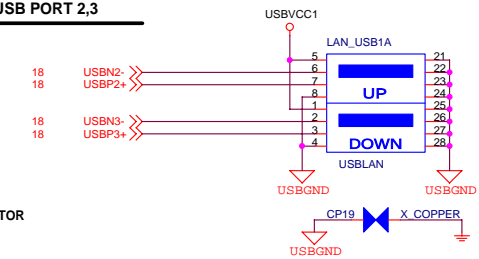
POWER CIRCUIT FOR USB PORT 0,1



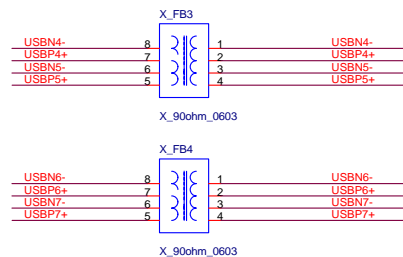
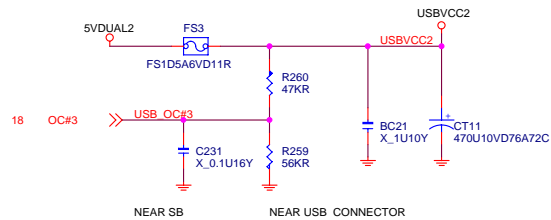
REAR PANEL USB CONNECTOR FOR USB PORT 0,1



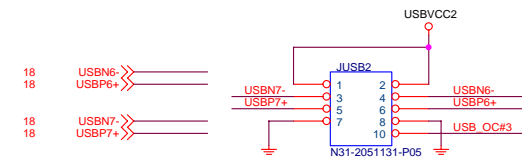
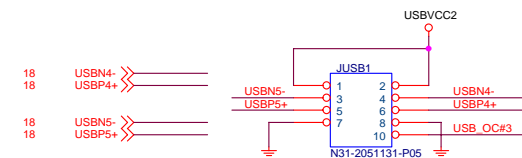
REAR PANEL USB CONNECTOR FOR USB PORT 2,3



POWER CIRCUIT FOR USB PORT 4,5

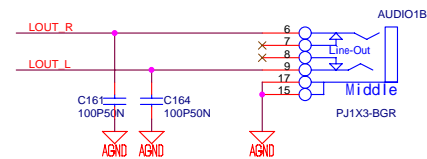
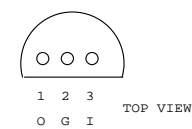


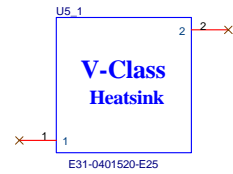
FRONT PANEL USB CONNECTOR FOR USB PORT 4,5



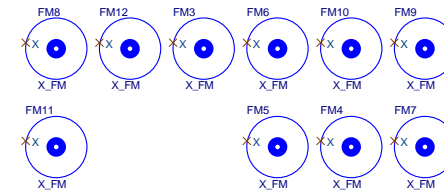
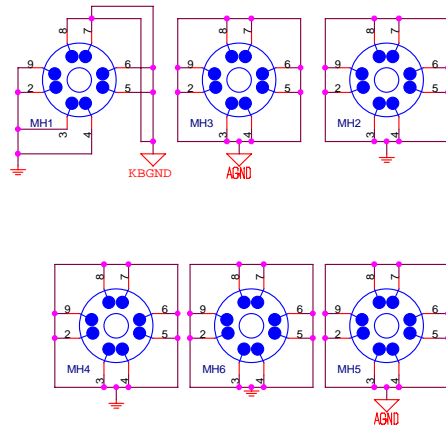
* USB Trace width : 7.5 mils
* USB Trace Spacing : 20 mils

* Differential USB Signlas Trace, Spacing : 7.5 mils
* USB Power Trace must be 50mils width

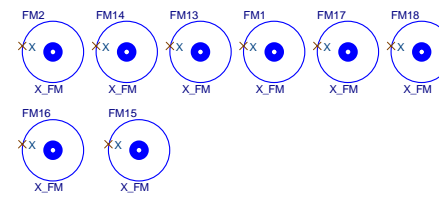




Mounting Holes



Optics Orientation Holes



Simulation

